REMARKS

Claims 1 – 14, 16 – 32 and 34 – 50 were pending in the application. By this paper, Applicant has amended Claims 1, 16, 23, 46, 48 and 50. Hence, Claims 1 – 14, 16 – 32 and 34 – 50 are presented for examination herein.

Amendments

Applicant has herein amended Claims 1, 16, 23, 46, 48 and 50 to correct an editorial defect (missing word "operation") to improve clarity and form. Applicant submits that this amendment is supported by the specification, and no new matter added.

Rejections under 35 U.S.C. §103

Claims 1, 13, 16, 23, 28, 45, 46, 48, 49, 50 – Traversal of "Official Notice"

By this paper, Applicant traverses all explicit and implicit "Official Notice" taken by the Examiner in the Office Action per, *inter alia*, MPEP 2144.03C.

(i) **Improper and Non-judicious use of Official Notice** - MPEP 2144.03 states in relevant part:

> *"In limited circumstances, it is appropriate for an examiner to take official notice of facts not in the record or to rely on "common knowledge" in making a rejection, however such rejections should be judiciously applied.*
> ...
> *The standard of review applied to findings of fact is the "substantial evidence" standard under the Administrative Procedure Act (APA). See In re Gartside, 203 F.3d 1305, 1315, 53 USPQ2d 1769, 1775 (Fed. Cir. 2000). See also MPEP § 1216.01.*

Applicant submits that the Examiner is respectfully misapplying and stretching the Official Notice he is taking to say it teaches something which it does not. For example, his references shown on, e.g., Page 2, Par. 5 of the Office Action may *arguendo* show that DRAM is greater density, etc. than SRAM, but this is a far cry from the assertions the Examiner is making in his rejections about what is taught by references such as Inagami. As pointed out in great

detail in prior responses and herein, one cannot simply substitute DRAM for the SRAM or other generic memory types shown in the prior art cited by the Examiner as the primary bases for his rejections. Significant adaptation and functionality which is not present in the prior art is required to make this substitution.

The Examiner fails to address or dispute this fact, or provide any basis for a "suggestion to combine", which is required under the patent law; he merely says that "*it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Inagami's main storage to be a DRAM array*". Applicant submits that if the Examiner's basis for "suggestion to combine" is that it is "very popular" and has "high density and low price" (see top of page 3 of the Office Action), then there is a strong disincentive to combine; namely, the foregoing adaptation required to replace the taught SRAM with DRAM. Stated differently, whatever benefits ostensibly provided by low cost or high density would be offset be the need to significantly revise and adapt the Inagami (4,881,168) architecture. By analogy, the Examiner is in effect saying that a biplane does not teach use of a jet engine, but jet engines are popular and provide benefits, and therefore it would have been obvious to put a jet engine on a biplane, thereby ignoring the fact that a complete revision of the biplane's structure would be needed to accommodate the jet engine in the first place. This cannot be rightfully said to be "suggestion to combine".

Hence, Applicant respectfully submits that the Examiner has rejected Applicant's claims on clearly improper grounds.

Applicant further submits that the Examiner of record has omitted or failed to provide support for one or more essential elements of each claim currently pending; i.e., the functional and structural adaptation to permit use DRAM versus other types of memory.

Further, the Examiner has explicitly utilized "Official Notice" as a basis of rejection in no less than **fourteen (14)** separate instances within the Office Action (**including at least once in each of all ten (10) independent claims presented, thereby causing Official Notice to be a substantive basis of all rejections of all claims, dependent and independent, previously presented**), and further has implicitly used Official Notice in numerous other instances (e.g., using the word "inherent" and variations thereof). Further, Applicant notes that the Examiner has used inherency type arguments based on elements non-existent within the references themselves,

essentially using inherency on elements which were added based on "Official Notice". Applicant submits that this cannot in any way be considered "judicious application" in "limited circumstances" as required by the MPEP.

(ii) **Improper Use of "Official Notice" as Principal Evidence of Obviousness** – In addition to the foregoing, the Examiner improperly uses such explicit or implicit Official Notice as a critical or principal basis of all of his rejections of the independent claims. Such Official Notice is improper and clearly not in accordance with MPEP 2144.03A&B; *"It is never appropriate to rely solely on "common knowledge" in the art without evidentiary support in the record, as the principal evidence upon which a rejection was based. Zurko,* 258 F.3d at 1385, 59 USPQ2d at 1697 {emphasis added}.

Also, as previously noted, the Examiner states the "DRAM and its advantages are well known and expected in the art", and that "DRAM is a very popular memory technology because of ...", but the Examiner provides no basis whatsoever for the proposition that DRAM is interchangeable with SRAM or any other generic memory of the type cited in his primary prior art references; this is because it is not in fact interchangeable with any other type of memory in Applicant's claimed inventions. The Examiner's repeated citation of Official Notice throughout the Action for the foregoing propositions comprises an improper use of Official Notice pursuant to MPEP 2144.03 A-C. Applicant's invention of, e.g., Claim 1 utilizes a specific optimized architecture including an embedded DRAM processor that interfaces directly to DRAM.

In the context of aforementioned analogy, the Official Notice of "a jet engine" is improperly used as the primary basis of the rejection, being "boot-strapped" to the bi-plane art to ostensibly teach or suggest something which it clearly does not (i.e., a jet aircraft with a jet engine).

Applicant also notes that *"[A] patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once the source of the problem is identified. This is part of the 'subject matter as a whole' which should always be considered in determining the obviousness of an invention under 35 U.S.C. § 103."* In re Sponnoble, 405 F.2d 578, 585, 160 USPQ 237, 243 (CCPA 1969). See MPEP 2141.02; *"The court found the inventor discovered the cause of moisture transmission was through the center plug, and there was no*

teaching in the prior art which would suggest the necessity of selecting applicant's plug material which was more impervious to liquids than the natural rubber plug of the prior art." **None of the art cited by the Examiner recognizes the problem Applicant's inventions seek to address. In the context of Applicant's analogy, none of the "bi-plane" art ever recognizes the need for a better propulsion source, or conversely the problems with a propellor engine arrangement**. This would be tantamount to Inagami stating that his own teachings were deficient or undesirable ("*well, despite the fact that I'm teaching using SRAM as my primary embodiment, it's really not the best choice...*"). This reasoning by the Examiner is specious on its face.

Claim 1 – Per paragraph 5 of the Office Action, Claim 1 stands rejected as being unpatentable over Inagami et al. (U.S. Patent No. 4,881,168, hereinafter "Inagami"). Applicant traverses. In addition to Applicant's objection to the Examiner's use of Official Notice as previously set forth, Applicant submits that Inagami does not teach "*a row address register that holds a pointer that points to a row of the DRAM array*". The citation by the Examiner in support of his assertion that such a limitation is taught by Inagami provides:

> "*Numeral 60 denotes a vector address register (VAR) group which comprises registers for holding main storage addresses (start addresses) of start elements of vector data in the main storage 1 or to be written into the main storage 1.*"

Applicant respectfully must disagree with the Examiner's assertion. While Inagami teaches start addresses of start elements of vector data, Inagami does not teach a pointer that points to a row of a DRAM array; Applicant requests the Examiner point to specific language that teaches a pointer that points to a row of the DRAM array.

Further, Applicant submits that Inagami does not teach or suggest "*a command to deactivate said row pointed to by said row address register after it had been precharged by the command to precharge*". See Par. 5 (iii) on page 3 of the Office Action. While it may or may not be inherent that if the rows are not deactivated they will stay activated as suggested by the Examiner, clearly this is not the same as a command to deactivate said row pointed to by said row address register after it had been pre-charged by the command to precharge as claimed by

Applicant. Applicant requests the Examiner point to specific language in Inagami that teaches "a command to deactivate".

In addition, Applicant submits that Inagami does not teach or suggest "*a command to load selected columns of the precharged row into designated sets of data registers, said selection based on bits in a mask.*" Inagami does not make any mention of any precharged rows; let alone a command to load selected columns of the precharged row, etc. Applicant is not sure whether the Examiner is attempting to combine the teachings of Wright et al. (U.S. Patent No. 5,587,961, hereinafter "Wright") with Inagami to come to the conclusion that the Examiner has reached. As the Examiner has not formally rendered Claim 1 unpatentable over Inagami in view of Wright, nor offered any rationale suggesting any motivation to combine these references, Applicant assumes that the Examiner believes that Inagami is the only reference needed to teach or suggest each and every limitation present in Claim 1.

Hence, Applicant submits that the Examiner's rejection of Claim 1 is improper as lacking at least three (3) different claimed elements or groupings of elements while improperly utilizing Official Notice and Inherency.

In addition, if the Examiner is attempting to combine the teachings of Wright with Inagami in order to render Applicant's invention obvious, Applicant submits that the Examiner has not met his *prima facie* burden in suggesting a motivation to combine the references and thus any attempted combination would be improper. **See e.g. MPEP 2143.**

Claim 13 – Per paragraph 12 of the Office Action, Claim 13 stands rejected as being unpatentable over Inagami et al. (US Patent No. 4,881,168, hereinafter "Inagami"). Applicant traverses. In addition to Applicant's objection to the Examiner's use of Official Notice as previously set forth, Applicant submits that Inagami does not teach "*a row address register that holds a pointer that points to a row of the DRAM array*". The citation by the Examiner in support of his assertion that such a limitation is taught by Inagami provides:

> "*Numeral 60 denotes a vector address register (VAR) group which comprises registers for holding main storage addresses (start addresses) of start elements of vector data in the main storage 1 or to be written into the main storage 1.*"

Applicant respectfully must disagree with the Examiner's assertion. While Inagami teaches start addresses of start elements of vector data, Inagami does not teach a pointer that points to a row of a DRAM array; hence Applicant requests that the Examiner point to specific language that teaches a pointer that points to a row of the DRAM array.

Applicant also traverses the Examiner's finding that Inagami teaches or suggests "*a command to precharge the row pointed to by said row address register*". The Examiner claims that this element is inherently taught by Inagami although Inagami does not teach or suggest DRAM or pre-charging. It is unclear to Applicant how a command to precharge the row pointed to by said row address register must necessarily be present when it requires Official Notice to show that Inagami could even be modified to be DRAM. Applicant believes such a rationale is clear error. Applicant respectfully brings to the attention of the Examiner the requirements under MPEP 2112, which provides in pertinent part, that:

> "*In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art.*" *Ex parte Levy,* 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original).

As the Examiner has already admitted that Inagami does not teach DRAM (see e.g. Page 7 of the Office Action), and Applicant does not believe Inagami teaches any sort of "precharging", the Examiner's use of an inherency argument is respectfully nonsensical and clear error. Clearly a precharging command is not necessarily inherent in the invention of Inagami.

Applicant also submits that Inagami does not teach or suggest "*a command to load a set of selected elements of the precharged row pointed to by said row address register into a selected set of said data registers, said selection based on bits in said bit mask*". Inagami does not teach or suggest or even mention the concept of precharged row and thus could not teach Applicant's claimed limitation as suggested by the Examiner.

Applicant also notes that the Examiner utilizes another inherency argument to suggest that Inagami somehow inherently teaches that "*the command to precharge is executed to precharge the row prior to the command to load so that at the time the command to load is*

issued, the command to load can execute without the need to wait for the row to precharge". Applicant believes this is improper for the reasons previously set forth.

Further, Applicant reiterates that if the Examiner is attempting to combine the teachings of Wright with Inagami in order to render Applicant's invention obvious, the Examiner has not met his *prima facie* burden in suggesting a motivation to combine the references and thus any attempted combination or modification would be improper. **See e.g. MPEP 2143.**

Claim 16 – Per paragraph 30 of the Office Action, Claim 16 stands rejected as being unpatentable over Inagami in view of Parady (U.S. Patent No. 5,933,627) and further in view of Bissett, et al. (U.S. Patent No. 5,896,523, hereinafter "Bissett"). Applicant respectfully traverses.

Specifically, Applicant submits that Inagami does not teach "an embedded DRAM array". The Examiner alleges that DRAM is well known and expected in the art and that memory inherently comprises rows and columns of memory cells. The Examiner also broadly construes the term "embedded", thus alleging that Inagami teaches an "embedded DRAM array". However, Applicant believes that the Examiner is improperly applying the legal standard for inherency among others. Applicant re-directs the Examiner's attention to MPEP 2112 which provides in pertinent part that:

> "*The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic....In relying upon the theory of inherency, the examiner **must** provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art.*"

Thus, Applicant submits that the Examiner has not provided a basis in fact and/or technical reasoning to support the determination that, *inter alia*, the memory of Inagami inherently or necessarily must comprise rows and columns as required. In fact, the main storage of Inagami could be construed to suggest a single column type structure (see e.g. Fig. 5). Regardless, Applicant submits that the Examiner has not met his burden in demonstrating that the memory of Inagami must necessarily comprise rows and columns.

In addition, Applicant submits that Inagami does not teach "*a row address register that holds a pointer that points to a row of the DRAM array*". The citation by the Examiner in support of his assertion that such a limitation is taught by Inagami provides:

> "*Numeral 60 denotes a vector address register (VAR) group which comprises registers for holding main storage addresses (start addresses) of start elements of vector data in the main storage 1 or to be written into the main storage 1.*"

Applicant respectfully must disagree with the Examiner's assertion. While Inagami teaches start addresses of start elements of vector data, Inagami does not teach a pointer that points to a row of a DRAM array; hence Applicant requests that the Examiner point to specific language that teaches a pointer that points to a row of the DRAM array.

Applicant submits that neither Inagami nor Parady nor Bissett teaches or suggests "*a command to load a set of selected elements of the row pointed to by said row address register into a selected set of said data registers, said selection based on bits in said bit mask, and the selected set of said data registers being in the inactive state.*" It is not clear in Applicant's view that the Examiner has addressed the claimed limitation. Specific terminology that may be pertinent to Bissett may have been used by the Examiner, but it is unclear how this addresses Applicant's claimed limitations of Claim 16. As the terminology is apparently mixed, i.e. Bissett is described without context to the applicable claim language, Applicant respectfully seeks clarification as to how the Examiner has equated the terminology in Bissett with specific terminology used by Applicant so that Applicant may properly address this rejection.

Claim 23 – Per paragraph 14 of the Office Action, Claim 23 stands rejected as being unpatentable over Inagami et al.. Applicant respectfully traverses. In addition to Applicant's objection to the Examiner's use of Official Notice as previously set forth, Applicant submits that Inagami does not teach "*a row address register that holds a pointer that points to a row of the DRAM array*". The citation by the Examiner in support of his assertion that such a limitation is taught by Inagami provides:

> *"Numeral 60 denotes a vector address register (VAR) group which comprises registers for holding main storage addresses (start addresses) of start elements of vector data in the main storage 1 or to be written into the main storage 1."*

Applicant respectfully must disagree with the Examiner's assertion. While Inagami teaches start addresses of start elements of vector data, Inagami does not teach a pointer that points to a row of a DRAM array; hence Applicant requests that the Examiner point to specific language that teaches a pointer that points to a row of the DRAM array.

Applicant also submits that Inagami does not teach or suggest "*a command to perform arithmetic (operation) on said row address register*". While Applicant agrees that the start address calculation unit 310 calculates the main storage addresses of the vector elements, it is not clear to Applicant that "a command" exists *per se,* that performs arithmetic operations on the row address register. Applicant requests the Examiner point to specific language which teaches "a command to perform arithmetic operations on said row address register".

Claims 28, 45, 49 and 50 – Per paragraphs 37, 53, 54 and 55 of the Office Action, Claims 28, 45, 49 and 50 stand rejected as being unpatentable over Inagami in view of Parady and further in view of Bissett. Applicant traverses, specifically, Applicant submits that these references do not teach "an embedded DRAM array". The Examiner alleges that DRAM is well known and expected in the art and that memory inherently comprises rows and columns of memory cells.

However, Applicant believes that the Examiner is improperly applying the legal standard for inherency as previously discussed. Applicant submits that the Examiner has not provided a basis in fact and/or technical reasoning to support the determination that, *inter alia*, the memory of Inagami necessarily must comprise rows and columns. In fact, the main storage of Inagami could be viewed to suggest a single column type structure (see e.g. Fig. 5). Regardless, Applicant submits that the Examiner has not met his burden in demonstrating that the memory of Inagami must necessarily comprise rows and columns.

Claim 46 – Per paragraph 18 of the Office Action, Claim 46 stands rejected as being unpatentable over Inagami. Applicant traverses. Applicant notes that the Examiner's arguments

are directed towards "speculative prefetching" (see Par. (ii) on page 13 of the Office Action); an element not present within Applicant's claimed language. Is the Examiner saying speculative prefetching equates with speculative precharging? As the Examiner has seemingly based arguments on an element not present within Applicant's claimed language, Applicant is unable to fully address the Examiner's substantive rejection of Claim 46 as the rejection in its current form is improper.

Claim 48 – Per paragraph 20 of the Office Action, Claim 48 stands rejected as being unpatentable over Inagami. Applicant traverses. Specifically, Applicant submits that saying an element is inherent in lieu of an element admittedly not taught by a reference is improper as previously set forth. Applicant submits that the Examiner has not met his *prima facie* burden in showing that an element is inherently taught (e.g. the act of precharging, etc.). Essentially, the Examiner is taking the view that any reference which teaches the generic concept of "memory" would render obvious the act of "precharging", an act which is limited to a subset of very specific memory architectures. Clearly this assertion by the Examiner cannot be correct and would not be in compliance with MPEP 2112.

Further, the Examiner is pointing towards the teachings of Wright in support of his position; however it appears that this reference is only being used as extrinsic evidence and not for the substantive teaching of individual elements within Applicant's claimed language. If the Examiner intends to say that Claim 48 is rendered obvious over Wright in view of Inagami, then the Examiner has a *prima facie* obligation to demonstrate a motivation or suggestion within the references themselves that demonstrates their ability to be combined or modified. As the Examiner has not done this, Applicant assumes the Examiner merely intends to use Inagami for the purpose of teaching the existence of each and every element present within Claim 48.

Other Remarks

Applicant hereby specifically reserves all rights of appeal, including those under the Pre-Appeal Brief Pilot Program, as well as the right to prosecute claims of different or broader scope in a continuation or divisional application.

Applicant notes that any claim cancellations or additions made herein are made solely for the purposes of more clearly and particularly describing and claiming the invention and responding to the aforementioned Action, and not for purposes of overcoming art or for patentability. The Examiner should infer no (i) adoption of a position with respect to patentability, (ii) change in the Applicant's position with respect to any claim or subject matter of the invention, or (iii) acquiescence in any way to any position taken by the Examiner, based on such claim cancellations or additions.

Furthermore, any remarks made with respect to a particular claim or claims shall be limited to only such claim or claims.

Respectfully submitted,

GAZDZINSKI & ASSOCIATES

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